In the Claims:

1. (Currently Amended) An apparatus for ensuring signal integrity of signals output from a latch, the apparatus comprising:

a first latch, the first latch having an input, an output and a latch enable;

a tri-state buffer having an input, an output and a drive enable;

a first conductive line connecting the input of the buffer to the output of the first latch;

a second latch, the second latch having an input, an output and a latch enable;

a second conductive line, the second conductive line being directly connected to the output of the buffer and to the output of the second latch, wherein when the drive enable is asserted, the buffer drives the output of the first latch such that signal integrity of the output of the first latch is ensured, and wherein when the driver enable is not asserted, the tri-state buffer exhibits high output impedance that isolates the second latch from the first latch.

2. (Original) A latch array comprising:

at least one column of latches, the column of latches comprising at least first, second and third sections, each latch of each section having an input, an output and a latch enable, the second section being located between the first and third sections in the column;

a first tri-state buffer comprised by the first section, the first tri-state buffer having an input, an output and a drive enable, each output of each latch of the first section being connected to a first conductive line, which is connected to the input of the first tri-state buffer; and

a second tri-state buffer comprised by the second section, the second tri-state buffer having an input, an output and a drive enable, each output of each latch of the second section being connected to a second conductive line, which is connected to the input of the second tri-state buffer, each output of each latch of the third section being connected to a third conductive line, the third conductive line being connected to the output of the second tri-state buffer.

3. (Original) The apparatus of claim 2, wherein when a latch in the first section is being addressed, the enables of the first and second tri-state buffers are asserted, and wherein asserting the enables of the first and second tri-state buffers causes the output of the latch being addressed to be driven by the first and second tri-state buffers.

4. (Original) The apparatus of claim 2, wherein when a latch in the second section is being addressed, the enable of the second tri-state buffer is asserted and the enable of the first tri-state buffer is de-asserted, and wherein de-asserting the enable of the first tri-state buffer causes the first tri-state buffer to exhibit high output impedance, which isolates the first section from the second and third sections, and wherein asserting the enable of the second tri-state buffer causes the output of the latch being addressed in the second section to be driven by the second tri-state buffer.

5. (Original) The apparatus of claim 2, wherein when a latch in the third section is being addressed, the enables of the first and second tri-state buffers are de-asserted, and wherein de-asserting the enables of the first and second tri-state buffers causes the first and second tri-state buffers to exhibit high output impedance, which isolates the third section from the first and second sections.

6. (Original) A latch array comprising:

at least one column of latches, the column of latches comprising sections 1 to N-1, N being a positive integer;

a plurality of latches comprised by each section, each latch of each section having an input, an output and a latch enable;

M tri-state buffers, M being a positive integer that is less than N, each of N-M of the sections comprising at least one of M tri-state buffers, and wherein the sections that comprise the tri-state buffers are each a sufficient distance away from an output of the column that a driving strength of the buffer of the section is needed to ensure signal integrity of signals output from the latches of the N-M sections.

7. (Original) The latch array of claim 6, wherein the latch array comprises a plurality of said columns of latches, the latch array being embedded in an integrated circuit (IC).

8. (Original) The latch array of claim 6, wherein when a latch of one of the sections of the column of latch arrays is being addressed, the tri-state buffer of the section comprising the latch that is being addressed is enabled and each tri-state buffer of the sections below the enabled tri-state buffer in the column are also enabled.

9. (Original) The latch array of claim 6, wherein when a latch of one of the sections of the column of latch arrays is being addressed, the tri-state buffer of the section comprising the latch that is being addressed is enabled and each tri-state buffer of the sections above the enabled tri-state buffer in the column are disabled.

10. (Currently Amended) A method for ensuring signal integrity of signals output from a latch, the method comprising the steps of:

providing a first latch having an input, an output and a latch enable; providing a tri-state buffer having an input, an output and a drive enable; connecting a first conductive line to the input of the buffer and to the output of

the first latch;

providing a second latch having an input, an output and a latch enable; connecting a second conductive line directly to the output of the buffer and to the output of the second latch, wherein when the drive enable is asserted, the buffer drives the output of the first latch such that signal integrity of the output of the first latch is ensured, and wherein when the drive enable is not asserted, the tri-state buffer exhibits high output impedance that isolates the second latch (24) from the first latch (21) and first conductive line.

11. (Original) A method for ensuring signal integrity of signals output from latches of a latch array, the method comprising the steps of:

providing at least one column of latches, the column of latches comprising at least first, second and third sections, each latch of each section having an input, an output and a latch enable, the second section being located between the first and third sections in the column;

providing a first tri-state buffer comprised by the first section, the first tri-state buffer having an input, an output and a drive enable, each output of each latch of the
first section being connected to a first conductive line, which is connected to the input of the first tri-state buffer; and

providing a second tri-state buffer comprised by the second section, the second tri-state buffer having an input, an output and a drive enable, each output of each latch of the second section being connected to a second conductive line, which is connected to the input of the second tri-state buffer, each output of each latch of the third section being connected to a third conductive line, the third conductive line being connected to the output of the second tri-state buffer.

12. (Original) The method of claim 11, wherein when a latch in the first section is being addressed, the enables of the first and second tri-state buffers are asserted, and wherein asserting the enables of the first and second tri-state buffers causes the output of the latch being addressed to be driven by the first and second tri-state buffers.

13. (Original) The method of claim 11, wherein when a latch in the second section is being addressed, the enable of the second tri-state buffer is asserted and the enable of the first tri-state buffer is de-asserted, and wherein de-asserting the enable of the first tri-state buffer causes the first tri-state buffer to exhibit high output impedance, which isolates the first section from the second and third sections, and wherein asserting the enable of the second tri-state buffer causes the output of the latch being addressed in the second section to be driven by the second tri-state buffer.

14. (Original) The method of claim 11, wherein when a latch in the third section is being addressed, the enables of the first and second tri-state buffers are de-asserted, and wherein dc-asserting the enables of the first and second tri-state buffers causes the first and second tri-state buffers to exhibit high output impedance, which isolates the third section from the first and second sections.

15. (Cancelled)
16. (Cancelled)
17. (Cancelled)
18. (Cancelled)
19. (Cancelled)
20. (Cancelled)